IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant:	Robin Alexis Takasugi et al.	Examiner: Sheng Jen Tsai
Serial No.:	10/672,975	Group Art Unit: 2186
Filed:	September 26, 2003	Docket No.: 10014268-1 / H303.154.101
Due Date:	**February 13, 2008** w/ extension	
Title:	PREFETCH CONTROLLER FOR CONTROLLING RETRIEVAL OF DATA FROM A DATA STORAGE DEVICE	

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Notification of Non-Compliant Appeal Brief mailed December 13, 2007, please consider the following remarks and the attached Revised Summary of Claimed Subject Matter:

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REVISED SUMMARY OF THE CLAIMED SUBJECT MATTER

The Summary is set forth as an exemplary embodiment as the language corresponding to independent claims 1, 12, 17, and 20, and dependent claim 19. Discussions about elements of claims 1, 12, 17, 19, and 20 can be found at least at the cited locations in the specification and drawings.

The present invention, as claimed in independent claim 1, provides a prefetch controller (Figure 1, reference number 104; specification at page 5, lines 1-14) for controlling retrieval of data from a data storage device (Figure 1, reference number 106) in response to a current host command received from a host device (Figure 1, reference number 102). The prefetch controller includes a sequential read detector (Figure 2, reference number 206; specification at page 7, line 29, to page 8, line 2) configured to generate a new sequential read indication for the current host command if the current host command and a previously received host command specify read operations that are non-sequential. A transfer length generator (Figures 1 and 4, reference number 118; specification at page 10, lines 13-26) is configured to provide a first transfer length value to the data storage device if the new sequential read indication is generated for the current host command, thereby requesting data specified by the current host command and prefetch data, and provide a second transfer length value to the data storage device if the new sequential read indication is not generated for the current host command. The first transfer length value is determined by adding a prefetch value to a transfer length value specified in the current host command. (See, e.g., specification at page 10, line 9 to page 11, line 10; Figures 1, 2, and 4; reference numbers 102, 104, 106, 116A-1, 118, and 206).

In addition to the above concise explanation, a more concise explanation of specific features can be found at, for example, the specification at page 11, lines 1-10. As set forth therein, during each command execution cycle, the prefetch length value output by multiplexer 408 and the transfer length value stored in register 414 are provided to adder 412, which adds the two received values, and outputs the sum to storage device interface 122 (Figure 1) via communication link 120A-1. The sum of the prefetch length value and the transfer length value represent the total transfer length value for the current host command. Thus, in one embodiment, for each READ command, a prefetch value is added by hardware

to the transfer length value specified in the READ command, with the prefetch value varying depending upon whether the transfer is a new sequential READ or not. (Specification at page 11, lines 1-10).

The present invention, as claimed in independent claim 12, provides a method of transferring data between a host electronic device (Figure 1, reference number 102) and a data storage device (Figure 1, reference number 106). The method includes receiving a current read command from the host electronic device. (Figure 6, reference numbers 602 and 604; specification at page 15, line 30, to page 16, line 7). The current read command specifies a first transfer length value. The method includes identifying whether the current read command is non-sequential to a previously received read command. (Figure 6, reference number 606; specification at page 16, lines 8-15). The method includes adding a prefetch length value to the first transfer length value if the current read command and the previous read command are non-sequential, thereby generating a second transfer length value. (Figure 6, reference number 610; specification at page 16, lines 22-25). The method includes outputting the second transfer length value to the data storage device. (See, e.g., specification at page 4, lines 10-16, and page 15, line 26 to page 17, line 5; Figures 1 and 6; reference numbers 102, 106, 602, 606, 610, and 614).

The present invention, as claimed in independent claim 17, provides a memory device including **storage means** (Figure 1, reference number 106; specification at page 4, lines 12-13) for storing data. The memory device includes **host interface means** (Figure 1, reference number 114; specification at page 5, lines 22-24) for receiving host commands from a host electronic device, **sequential read detection means** (Figure 2, reference number 206; specification at page 7, line 29 to page 8, line 2) for identifying whether a current host command specifies a non-sequential read operation, and **transfer length generation means** (Figures 1 and 4, reference number 118; specification at page 10, lines 13-26) for adding a prefetch length value to a transfer length value specified in the current host command if the current host command specifies a non-sequential read operation. The transfer length generation means is configured to output a sum of the prefetch length value and the transfer length value to the storage means. (See, e.g., specification at page 10, line 9 to page 11, line 10; Figures 1, 2, and 4; reference numbers 102, 104, 106, 114, 118, and 206).

In addition to the above concise explanation, a more concise explanation of specific features can be found at, for example, the specification at page 11, lines 1-10. As set forth therein, during each command execution cycle, the prefetch length value output by multiplexer 408 and the transfer length value stored in register 414 are provided to adder 412, which adds the two received values, and outputs the sum to storage device interface 122 (Figure 1) via communication link 120A-1. The sum of the prefetch length value and the transfer length value represent the total transfer length value for the current host command. Thus, in one embodiment, for each READ command, a prefetch value is added by hardware to the transfer length value specified in the READ command, with the prefetch value varying depending upon whether the transfer is a new sequential READ or not. (Specification at page 11, lines 1-10).

The present invention, as claimed in dependent claim 19, provides the memory device of claim 17, wherein the transfer length generation means comprises: **first register means** (Figure 4, reference number 404; specification at page 10, lines 11-12) for storing the prefetch length value; **second register means** (Figure 4, reference number 406; specification at page 10, line 13) for storing a zero value; **multiplexing means** (Figure 4, reference number 408; specification at page 10, lines 13-26) for selectively outputting the prefetch length value or the zero value based on an output of the sequential read detection means; and **adding means** (Figure 4, reference number 412; specification at page 11, lines 1-5) for adding an output of the multiplexing means and the transfer length value specified in the current host command. (See, e.g., specification at page 10, line 9 to page 11, line 10; Figures 1, 2, and 4; reference numbers 102, 104, 106, 114, 118, 206, 404, 406, 408, and 412).

In addition to the above concise explanation, a more concise explanation of specific features can be found at, for example, the specification at page 10, lines 13-26. As set forth therein, during each command execution cycle, the values stored in registers 404 and 406 are both provided to multiplexer 408, which outputs one of the two values to adder 412 based on a signal received on communication link 116A-1 from sequential read logic 308 (Figure 3). In one embodiment, if sequential read logic 308 outputs a logically true new sequential read flag for the current host command to multiplexer 408 via communication link 116A-1, multiplexer 408 outputs the value stored in prefetch register 404 to adder 412. If sequential

read logic 308 outputs a logically false new sequential read flag for the current host command to multiplexer 408 via communication link 116A-1, multiplexer 408 outputs the value stored in zero register 406 to adder 412. Thus, the signal output by sequential read logic 308 selectively switches the multiplexer 408 to output either a non-zero prefetch value in the case of a potentially new sequential transfer, or a zero if the current transfer is not a new sequential transfer. (Specification at page 10, lines 13-26).

The present invention, as claimed in independent claim 20, provides a computer-readable medium having computer-executable instructions for performing a method of transferring data between a host electronic device (Figure 1, reference number 102) and a data storage device (Figure 1, reference number 106). The method includes receiving a current host command from the host electronic device (Figure 6, reference numbers 602 and 604; specification at page 15, line 30, to page 16, line 7), generating a new sequential read indication (Figure 3, reference number 116A-1; specification at page 9, lines 18-25) for the current host command if the current host command and a previously received host command specify read operations that are non-sequential, and outputting a first transfer length value (Figure 6, reference number 614; specification at page 16, lines 28-30) to the data storage device if the new sequential read indication is generated for the current host command. The first transfer length value is determined by adding a prefetch value to a transfer length value specified in the current host command. (Figure 6, reference number 610; specification at page 16, lines 22-25). The method includes outputting a second transfer length value to the data storage device if the new sequential read indication is not generated for the current host command. (Figure 6, reference number 614; specification at page 16, lines 28-30). The second transfer length value is less than the first transfer length value. (See, e.g., specification at page 4, lines 10-16, and page 15, line 26 to page 17, line 5; Figures 1, 2, and 6; reference numbers 102, 106, 116A-1, 602, 606, 608, 610, and 614).

REMARKS

Comments Regarding Revised Summary

The Examiner stated in the Notification of Non-Compliant Appeal Brief mailed on December 13, 2007 that:

> The appeal brief fails to provide a consise (sic) explanation of the subject matter defined in each of the independent claims involved in the appeal.
>
> The summary provided for claims 17 and 19 are in compliance. However, the summary provided for claims 1, 12 and 20 fails to map the column, line numbers and figures to the specific elements recited in the claims. The summary provided for claims 1, 12 and 20 should follow the same format (i.e., to map the column, line numbers and figures to the specific elements recited in the claims) as in claims 17 and 19. (Notification at page 2).

Appellant respectfully disagrees with the Examiner's argument in the Notification that claims 1, 12, and 20 are non-compliant because these claims do not include a mapping for specific elements. Applicant could find no such specific element mapping requirement in 37 CFR § 41.37(c)(1)(v), or any other rule or statute. Rather, 37 CFR § 41.37(c)(1)(v) specifies that:

> *Summary of claimed subject matter.* A concise explanation of the subject matter defined in each of the independent claims involved in the appeal, which shall refer to the specification by page and line number, and to the drawing, if any, by reference characters. For each independent claim involved in the appeal and for each dependent claim argued separately under the provisions of paragraph (c)(1)(vii) of this section, **every means plus function and step plus function as permitted by 35 U.S.C. 112, sixth paragraph, must be identified** and the structure, material, or acts described in the specification as corresponding to each claimed function must be set forth with reference to the specification by page and line number, and to the drawing, if any, by reference characters. (bold emphasis added)

The above rule indicates that there is a mapping requirement for means plus function limitations. However, the above rule does not specify that all elements, including non-means-plus-function elements, must be separately mapped to the specification as argued by the Examiner. Appellant is not aware of any means plus function or step plus function limitations under 35 U.S.C. § 112, sixth paragraph, in claims 1, 12, and 20 of the present

application. The Examiner has not identified any rule or statute that requires that elements in these independent claims must be separately mapped to the specification.

Even though Appellant is unaware of any requirement to provide the mapping identified by the Examiner, to hopefully facilitate progress of the present Appeal, Appellant has submitted herewith a Revised Summary of Claimed Subject Matter pursuant to MPEP § 1205.03 to address the mapping issue identified by the Examiner.

CONCLUSION

Any inquiry regarding this Response should be directed to either Nathan Rieth at Telephone No. (208) 396-5287, Facsimile No. (208) 396-3958 or Jeff A. Holmen at Telephone No. (612) 573-0178, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

Revised Appeal Brief
Applicant: Robin Alexis Takasugi et al.
Serial No.: 10/672,975
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Docket No.: 10014268-1 / HB03.154.101
Title: PREFETCH CONTROLLER FOR CONTROLLING RETRIEVAL OF DATA FROM A DATA STORAGE DEVICE

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Respectfully submitted,

Robin Alexis Takasugi et al.

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Dated: 2/5/08
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Jeff A. Hollmen
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CERTIFICATE UNDER 37 C.F.R. 1.8:

The undersigned hereby certifies that this paper or papers, as described herein, are being transmitted via telefacsimile to Fax No. (571) 273-8300 on this 5th day of February, 2008.

By: _____
Name: Jeff A. Hollmen